Amendments To the Claims:

Please amend the claims as shown. Applicants reserve the right to pursue any cancelled claims at a later date.

1.-11. (cancelled)

12. – 22. (cancelled)

23. (New) A method of combining and presenting output signals of a hardware simulation device and elements of a listing of a software program, comprising:

creating a program list file from a software program comprising a list of elements representing the sequence of the software program, wherein the elements comprise program commands and any associated comments;

running a hardware simulation of a circuit described in a hardware description language (HDL) in accordance with an input data file compiled from the software program as simulation code to obtain output signals;

receiving the output signals from the hardware simulation and the elements from the program list file in a debugger;

coupling by the debugger output signals and elements that correspond;

displaying a combined representation of the output signals and the elements by displaying in a first area of a display the list of elements representing the sequence of the software program and displaying in a second area of the display the output signals from the hardware simulation; and

synchronizing a first visual marking of a selected element in the first area with a second visual marking of a corresponding output signal in the second area based on the coupling by the debugger.

24. (New) The method in accordance with Claim 23, further comprising displaying at least a part of the output signals in a third area of the display.

25. (New) The method in accordance with Claim 24, wherein the output signals displayed in the second area comprise waveforms and the output signals displayed in the third area comprise register values.

26. (New) The method in accordance with Claim 23, further comprising selectively single stepping through a waveform in the second area representing the output signals corresponding to the elements representing the sequence of the software program.

27. (New) The method in accordance with Claim 26, wherein the single stepping comprises:

(a) determining a current simulation time from a value of a program counter of the output signal;

(b) advancing through the waveform until a change in the program counter occurs;

(c) placing the second visual marking on the waveform at a point where an executable command is reached or an end of the simulation is reached, and synchronizing the first visual marking in the first area; otherwise returning to step (b).

28. (New) A system for combining and representing signals of a hardware simulation device and elements of a listing of a software program, comprising:

a software program having program code stored in a memory of a circuit;

a hardware simulation device for running a hardware simulation of the circuit described in a hardware description language (HDL) in accordance with an input data file compiled from the software program as simulation code to obtain output signals;

a program list file from the software program comprising a list of elements representing the sequence of the software program, wherein the elements comprise program commands and any associated comments;

a debugger for receiving the output signals from the hardware simulation and the elements from the program list file and coupling output signals and elements that correspond;

a graphical display for displaying a combined representation of the output signals and the elements, comprising a first area for displaying the list of elements representing the sequence of the software program and a second area for displaying the output signals from the hardware simulation; and

a marking unit for synchronizing a first visual marking of a selected element in the first area with a second visual marking of a corresponding output signal in the second area based on the coupling by the debugger.

29. (New) The system in accordance with Claim 28, wherein the graphical display further comprises a third display area for displaying at least a part of the output signals.

30. (New) The system in accordance with Claim 29, wherein the output signals displayed in the second area comprise waveforms and the output signals displayed in the third area comprise register values.

31. (New) The system in accordance with Claim 28, wherein the debugger further comprises procedures for selectively single stepping through a waveform in the second area representing the output signals corresponding to the elements representing the sequence of the software program.

32. (New) The system in accordance with Claim 31, wherein the single stepping comprises:

(a) determining a current simulation time from a value of a program counter of the output signal;

(b) advancing through the waveform until a change in the program counter occurs;

(c) placing the second visual marking on the waveform at a point where an executable command is reached or an end of the simulation is reached, and synchronizing the first visual marking in the first area; otherwise returning to step (b).